A 1.8-V 6/9-GHz Switchable Dual-Band Quadrature LC VCO in SiGe BiCMOS Technology

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Abstract — **This paper presents a quadrature VCO that can be reconfigured between 6 and 9 GHz frequency bands. The dual-band VCO comprises a 6-GHz LC VCO, two 1/2-dividers, two mixers, and two 3-GHz notch filters. The 9-GHz output is generated based on a fractional frequency multiplication method by mixing the 6-GHz VCO output with its divide-by-two signal. The VCO, implemented in a 0.18-μm SiGe BiCMOS technology, shows a fast switching time of 3.6 nsec. The measured VCO phase noises are –106 dBc/Hz and -104 dBc/Hz at 1 MHz offset for 6 and 9-GHz modes, respectively, while draining 10.8 mA from a 1.8-V supply.**

I. INTRODUCTION

One of the major difficulties in implementing a dual-band transceiver is a voltage-controlled oscillator, because most VCO's are not capable of providing the most essential feature for a dual band application, that is, an agile reconfiguration between dual bands. A regenerative frequency multiplication method [1,2] is effective for generation of two fractionally separated frequencies, and there have been reports of using this method to generate RF-carriers at GHz range for a dual-band GSM [2] and a bluetooth transceiver [3]. Their purpose, however, was only to take advantage of a fractional offset between the VCO and the RF carrier frequency to suppress dc-offset and injection pulling in the intended direct conversion architecture. No switching characteristics were reported yet to date.

This paper presents a design of a dual-band quadrature LC VCO that is switchable between 6 and 9-GHz bands by using the frequency multiplication method. The dual-band VCO is developed in order to support our dual-band direct conversion receiver (shown in Fig. 1) with a reconfigurable aperture antenna [4].

II. ARCHITECTURE

The architecture of the dual-band switchable VCO is illustrated in Fig. 2. The chip comprises a 6-GHz quadrature LC VCO, two divide-by-two circuits, two mixers, and two 3-GHz notch filters. While only one divide-by-two circuit is used to drive the mixers, a divide-by-two circuit is connected to each I/Q node in the 6-GHz VCO in order to impose equal loading to the I and Q branches. These divide-by-two circuits accept the signal at f_{VCO} from the LC VCO and generate either a half-frequency signal ($f_{VCO}/2$) or a dc voltage, depending on the band selected. The mixers then generate outputs at frequencies of either ($3/2 \times f_{VCO}$) or f_{VCO}. Due to the nonlinearity in the mixing operation, many unwanted spurious tones exist in the ($3/2 \times f_{VCO}$)-output. To remove the frequency component especially at $f_{VCO}/2$, either a single-sideband mixer (SSBM) or a notch filter can be used. However, the high linearity requirements of a SSBM result in an unacceptably high-power design. Instead, we employed a notch filter from on-chip inductors and capacitors. The wide separation of f_{VCO} and $f_{VCO}/2$ enables the LC filter to give a reasonably high rejection even with a modest Q factor.

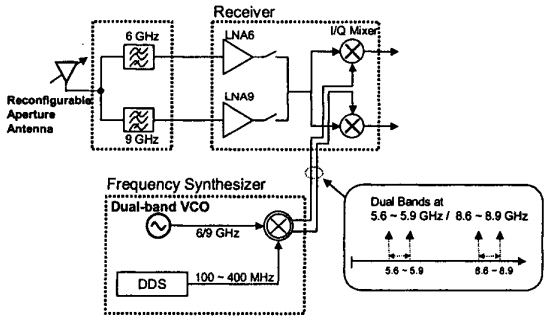

Figure 1. Architecture of the 6/9-GHz dual band direct conversion receiver

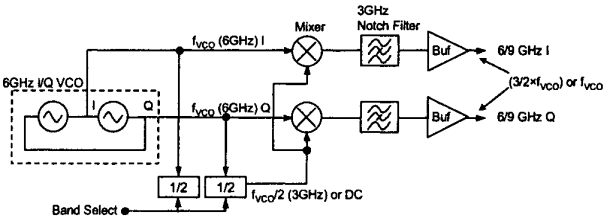

Figure 2. Architecture of the 6/9-GHz switchable dual-band VCO

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III. CIRCUIT DESIGN

There are several methods to generate a quadrature output in VCO. A RC-CR poly phase network is very difficult to implement in the 6-9 GHz frequency range. This is because the required resistances and capacitances are so small at such high frequencies that their ratio is difficult to control within an acceptable range. A quadrature output taken from a divide-by-two circuit requires a double frequency oscillator, which then requires a higher-frequency technology than is needed on the rest of the chip. Thus, we employed the ring-type quadrature LC VCO as shown in Fig. 3, where the three pairs of shaded blocks indicate the LC-resonator, the core cross-coupled transistors for negative resistance, and the driving transistors for I/Q generation. The bias currents for core and driving stages are denoted as I_C and I_D, respectively. The capacitive voltage divider of C_1 and C_2 is for dividing the feedback voltage from collector to base and thereby optimizing the loop gain.

In our design, I_C is set to be 1.8 mA for each VCO core, and I_D is set to 300 μA for the driving stage. G_{MD}/G_{MC} is thus set to 1/6, which is large enough to maintain the quadrature phase relation between I/Q as well as suppress any significant mismatch effects between the branches. Another design consideration is that the spiral inductor in the resonator is designed as large as practically possible, which is generally desirable for low phase noise performance. Here we used a 1.6-nH 3-turn spiral inductor and a varactor diode with 350-fF capacitance. The resonator Q-factor is approximately 12 at 6 GHz.

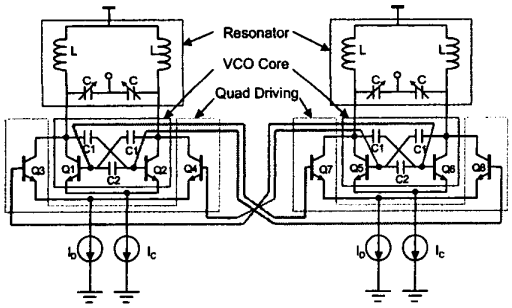

Figure 3. Circuit schematic of the quadrature LC VCO

A master-slave-type D flip-flop (MS-DFF) is used for the divide-by-two circuit because of its potential high speed characteristics. The simplified circuit schematic is shown in Fig. 4. Note that it includes switching circuitry between the $f_{VCO}/2$ and dc signals depending on the band selection. The band selection switch enables or disables the bias currents for the corresponding blocks. The dc voltage is created by a V_{offset} applied to the differential pair switch (Q7-8). I_o and the logic swing is designed to be 500 μA and 150mV ($6V_T$), respectively. The self-oscillation frequency of this divider is designed slightly higher than the operating frequency (f_{VCO}) so that the input sensitivity can be maximized and consequently the current consumption is minimized. The simulation shows that the input referred self-oscillation frequency is around 7.5 GHz.

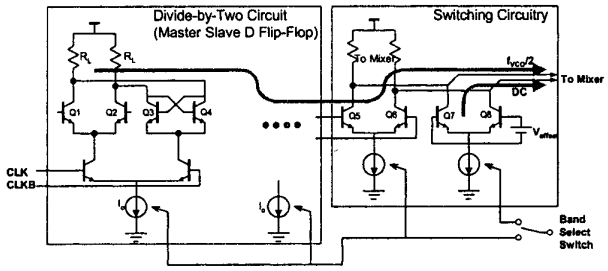

Figure 4. Circuit schematic of the divide-by-two circuit including switch circuitry

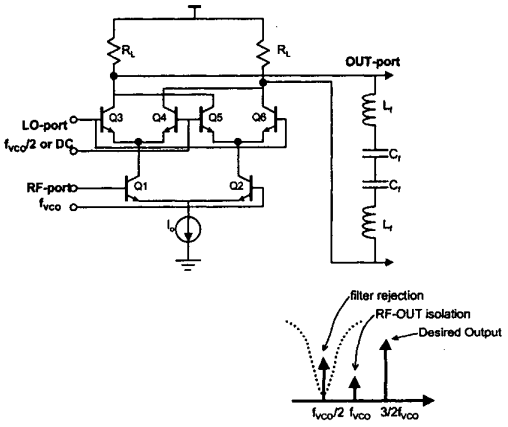

Figure 5. Circuit schematic of the Gilbert-cell mixer and LC notch filter

The circuit schematic of a Gilbert-cell mixer and a LC notch filter is shown in Fig. 5. f_{VCO} is applied to the RF-port and $f_{VCO}/2$ is applied to the LO-port. The quad (Q3-6) becomes a cascode connection when DC voltage is applied to the LO port. With an input of $f_{VCO}/2$, the output spectrum contains all the harmonics of $f_{VCO}/2$. The spectrum in the figure illustrates the three important frequency components; of which $3/2 \times f_{VCO}$ is the desired output and the other two components should be removed. The suppression of f_{VCO}-component is achieved by the inherent RF-OUT isolation characteristics of a Gilbert cell, which is designed to be about 30 dBc. On the other hands, the $f_{VCO}/2$ signal should have the

same magnitude as the $3/2\times f_{VCO}$ signal because the mixer inherently produces double sideband outputs. The $f_{VCO}/2$ signal is suppressed using a single-pole series LC notch filter. To make this filter, we choose $L_f = 3$ nH and $C_f = 0.9$ pF. The filter then resonates at 3 GHz with a Q-factor of around 15. Simulations show about 20 dB of rejection at 3-GHz compared to 6 and 9 GHz. Since there are two differential-output mixers for I/Q path, four notch filters are incorporated. A 4.5-turn inductor occupies 0.2×0.2 mm^2, so the four filters occupy almost 0.5×0.5 mm^2, which is almost 40 % of the real chip area. Area consumption thus limited our choice of filter order to 1. However, it is possible to use an off-chip filter to further remove the $f_{VCO}/2$-component in the final synthesizer implementation.

We simulate the switching behavior of the VCO. Fig. 6 shows the time domain simulation results carried out by using SpectreRF. Depending on the band selection, the VCO final output frequency is switching from 9-GHz to 6 GHz. The transition time is about 4 nsec.

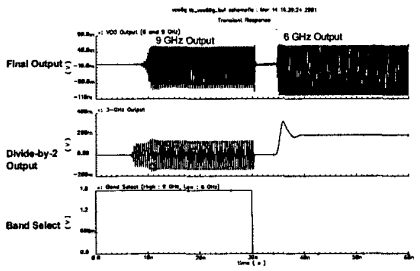

Figure 6. Simulation results of the switching behavior in VCO

IV. MEASUREMENT RESULTS

The VCO has been fabricated in a 0.18 μm SiGe BiCMOS technology which provides bipolar transistors with f_T and f_{MAX} of about 100-GHz, on-chip spiral inductors with a Q factor around 15, MIM capacitors, and accumulation-mode MOS varactor diodes. Fig. 7 shows a microphotograph of the fabricated chip. The chip area is 1.1×1.5 mm^2, including the output driving buffers and pads. The chip is tested at a 1.8-V supply and operated as low as 1.6 V. It was measured on-wafer by using a microwave probe.

VCO tests demonstrate successful switching behavior between the two modes. To compare the output spectrum of the two operation modes, the two spectrum measurement results are plotted together on the same scale in Fig. 8. The 6-GHz mode creates a fundamental signal at 6 GHz, a second harmonic at 12 GHz, and so on. On the other hand, the 9-GHz mode generates fundamental components at 9 GHz ($3/2\times f_{VCO}$), but also spurious outputs at 3 GHz ($f_{VCO}/2$) and 6 GHz (f_{VCO}). Note that notch filter rejection is measured to be far smaller than the designed 20-dBc. This is because the output is measured through a nonlinear output buffer amplifier for 50-Ω driving, which actually has higher gain at 3 GHz than at 9 GHz. The harmonic suppression between the f_{VCO} and $(3/2\times f_{VCO})$ signals, which is obtained by the RF-OUT isolation of the mixer, is measured at 22 dBc. It is also worse than the simulated 30 dBc because of the output buffer nonlinearity.

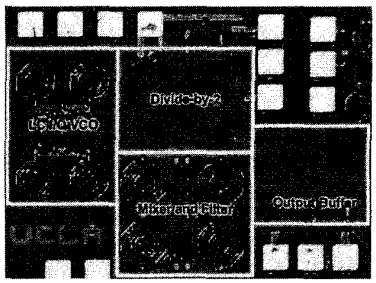

Figure 7. Chip micrograph

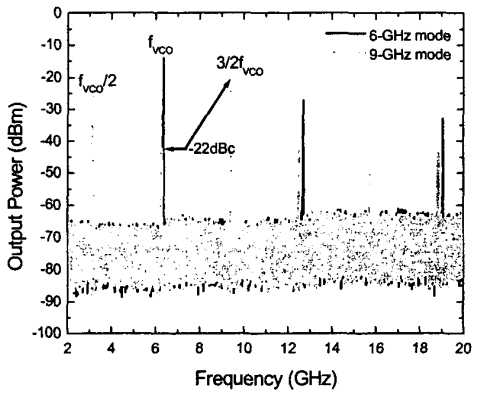

Figure 8. Spectrum measurement of 6-GHz and 9-GHz outputs

The frequency tuning characteristics are measured to be 300 MHz and 450 MHz for the 6 and 9-GHz modes, respectively. The 3/2-relationship is maintained for both modes, as expected. The phase noises are measured under the free-running condition by using a spectrum analyzer. They are -106 and -104 dBc/Hz at 1-MHz offset for the 6 and 9-GHz modes, respectively. VCO-FOM (figure of merit) is calculated by using the equation,

$$VCO-FOM = L_{meas}(f_{offset}) - 20\cdot log(f_{osc}/f_{offset}) + 10\cdot log(P_{diss}/1mW)$$

The VCO-FOMs of −176.7 and −178.2 dBc/Hz are obtained for the 6-GHz and 9-GHz modes, respectively. These are quite good figures compared to previous results in a similar frequency region [5].

The switching behavior has been measured in the time domain. Usually it is not possible to measure a time-domain

waveform of a free-running VCO at this high frequency region. This is because a high-speed sampling oscilloscope requires an additional triggering signal, which is not usually available from a free-running VCO. Since our interest is only the switching behavior between the two modes, we use a pulse generator to provide both the band select signal to the VCO and the triggering signal to the sampling oscilloscope at the same time. Fig. 9 shows the measurement results when the switching signal frequency is 5 MHz. Since the triggering is obtained only for the switching signal and not for the VCO output, the measured waveform cannot show a periodic sine-wave-like form. Thus, these regions are hatched out in the figure. However, the transition bands are nonetheless clearly differentiated. Fig. 9(a) is a close view of the switching from the 9-GHz mode to the 6-GHz mode. It shows clearly the VCO output frequency is switched seamlessly and quickly between the two modes. The measured transition time is 3.6 nsec, which shows a good agreement with the simulation. Fig. 9(b) shows a wider view of the input switching signal and the VCO output signal. The latency between the switching signal input and the actual VCO output change comes from the delay of many inverters at the digital pad. Simulations show that the internal latency is only 2 nsec.

Table I summarizes the measured VCO performance and power consumption. The total power consumption is 19.4 mW for all building blocks except the 50-Ω driving buffer amplifiers.

V. CONCLUSION

A switchable VCO at 6/9-GHz bands has been developed based on the fractional frequency multiplication method. It is comprised of a 6-GHz LC VCO, two divide-by-two circuits, two mixers, and two notch filters. The fabricated chip showed a fast reconfiguration time of 3.6 nsec between the 6 and 9-GHz operation modes.

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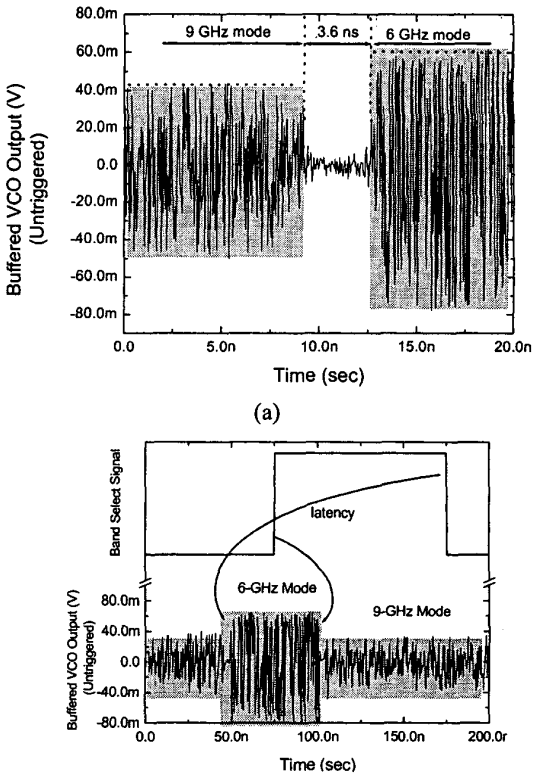

Figure 9. Transient measurement of switching behavior. Switching between the modes is achieved in 3.6 nsec

Table I. VCO Performance

Parameters	Performance
Supply Voltage	1.8V
Current Consumption	
- VCO core	1.8 mA
- Divide-by-2	2.0 mA
- Mixer	0.6 mA
- Total including I/Q paths	10.8 mA
Phase Noise @ 1 MHz offset	
- 6 GHz output	-106 dBc/Hz
- 9 GHz output	-104 dBc/Hz
- VCO FOM	-176 dBc/Hz
Tuning Range	300MHz / 6GHz 450MHz / 9GHz
Swithching Time	3.6 nsec